EAST SEARCH

8/23/05

L#	Hits	Search String	Databases
S1	4602	(((integrated or digital) near2 circuit$1) or "logical unit") with simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	25	S1 and (simulat$3 with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	39	S1 and (execut$3 with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	32	logical unit with simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	4	S1 and (thread$1 with manager$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	17	S1 and (resource$1 with manager$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	14	S1 and ((sequential$2 or concurrent$2) with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	82	S1 and (allocat$3 with resource$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	6	S1 and (allocat$3 with rule$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	15	S1 and (resource$1 with hierarch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	34	S1 and (monitor$3 with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	3	S1 and (request$1 with deadlock$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	1	S1 and (monitor$3 with (read or write) with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	136	S1 and (monitor$3 with (read or write))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	104	S1 and ((read or write) with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	47	S14 and S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	1	S1 and (competition with (read or write))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	0	S1 and (compet$3 with (read or write))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	26	S1 and (resource$3 with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	82	S1 and (number with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	52	S1 and (block$3 with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	301	S1 and (time with (occupancy or use or utilization))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	220	S1 and (time with resource)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	41	S22 and S23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	3	S1 and (thread$1 with "execution time")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	5	S1 and (limit$1 with "execution time")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	324	S1 and (compar$4 with result$1 with simulat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	215	S1 and (compar$4 with result$1 with output$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	102	S27 and S28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	27	S1 and (thread$1 with control$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	234	S4 or (S2 or S3 or S5 or S6 or S7 or S9 or S10 or S11 or S12 or S16 or S17 or S19 or S21 or	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	249	S8 or S20 or S29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	70	S31 and S32	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	234	S31 or S33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	4602	(((integrated or digital) near2 circuit$1) or "logical unit") with simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	25	S35 and (simulat$3 with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S37	39	S35 and (execut$3 with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S38	32	logical unit with simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S39	4	S35 and (thread$1 with manager$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	82	S35 and (allocat$3 with resource$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	6	S35 and (allocat$3 with rule$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	15	S35 and (resource$1 with hierarch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	34	S35 and (monitor$3 with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	3	S35 and (request$1 with deadlock$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	136	S35 and (monitor$3 with (read or write))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	104	S35 and ((read or write) with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	47	S47 and S48	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S50	1	S35 and (competition with (read or write))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	26	S35 and (resource$3 with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	82	S35 and (number with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	52	S35 and (block$3 with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	301	S35 and (time with (occupancy or use or utilization))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	220	S35 and (time with resource)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	41	S54 and S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S59	324	S35 and (compar$4 with result$1 with simulat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S60	215	S35 and (compar$4 with result$1 with output$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S61	102	S59 and S60	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S62	27	S35 and (thread$1 with control$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S63	234	S38 or (S36 or S37 or S39 or S40 or S41 or S43 or S44 or S45 or S46 or S49 or S50 or S51	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S64	249	S42 or S52 or S61	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S65	70	S63 and S64	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S41	14	S35 and ((sequential$2 or concurrent$2) with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S67	10	S35 and ((sequential$2 or serial$2) with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S66	234	S63 or S65	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S40	17	S35 and (resource$1 with manager$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S68	40	S35 and (arbiters or arbitrators)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S69	24	**S68 and (hierarch$6)**	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S70	2	S35 and ((arbitrat$3 or arbiter$1) with hierarch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S71	36	S35 and ((arbitrat$3 or arbiter$1) with (plurality or multiple))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S72	22	S66 and bottleneck$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S73	5	S66 and (blocking with (resource$1 or device$1 or request$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	3	S35 and (thread$1 with "execution time")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	5	S35 and (limit$1 with "execution time")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S74	5032	(((integrated or digital) near2 circuit$1) or "logical unit") with simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S75	28	S74 and (simulat$3 with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S76	47	S74 and (execut$3 with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S77	33	logical unit with simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S78	4	S74 and (thread$1 with manager$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S79	17	S74 and (resource$1 with manager$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S80	16	S74 and ((sequential$2 or concurrent$2) with thread$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S81	89	S74 and (allocat$3 with resource$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S82	6	S74 and (allocat$3 with rule$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S83	21	S74 and (resource$1 with hierarch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S84	38	S74 and (monitor$3 with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S85	3	S74 and (request$1 with deadlock$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S86	148	S74 and (monitor$3 with (read or write))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S87	114	S74 and ((read or write) with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S88	48	S86 and S87	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S89	1	S74 and (competition with (read or write))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S90	31	S74 and (resource$3 with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S91	87	S74 and (number with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S92	58	S74 and (block$3 with request$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S93	316	S74 and (time with (occupancy or use or utilization))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S94	241	S74 and (time with resource)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S95	43	S93 and S94	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S96	3	S74 and (thread$1 with "execution time")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S97	5	S74 and (limit$1 with "execution time")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S98	361	S74 and (compar$4 with result$1 with simulat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S99	234	S74 and (compar$4 with result$1 with output$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S100	107	S98 and S99	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S101	29	S74 and (thread$1 with control$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S102	258	S77 or (S75 or S76 or S78 or S79 or S80 or S82 or S83 or S84 or S85 or S88 or S89 or S90	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S103	266	S81 or S91 or S100	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S104	75	S102 and S103	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S105	258	S102 or S104	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S106	3	S105 and ((dynamic$4 near2 (assign$4 or allocat$3)) with (resource$1 or hardware))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S107	863	simulat$3 with (thread$1 or "logical unit")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S108	86	S107 and ((assign$4 or allocat$3) with (resource$1 or hardware))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S109	8	S108 and ((dynamic$4 near2 (assign$4 or allocat$3)) with (resource$1 or hardware))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

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Results of search set S115

Document Kind Codes	Title	Issue Date	Current OR	Abstract
US 20050172107 A1	Replay instruction morphing	20050804	712/226	
US 20050165597 A1	Apparatus and method for performing hardware and software co-verification testing	20050728	703/27	
US 20050151562 A1	Apparatus and method for bus signal termination compensation during detected quiet cycle	20050714	326/30	
US 20050120012 A1	Adaptive hierarchy usage monitoring HVAC control system	20050602	707/3	

US 20050108667 A1	METHOD FOR DESIGNING AN INTEGRATED CIRCUIT HAVING MULTIPLE VOLTAGE DOI	20050519	716/4
US 20050108039 A1	Semiconductor intellectual property technology transfer method and system	20050519	705/1
US 20050102125 A1	Inter-chip communication system	20050512	703/14
US 20050097551 A1	Multi-threaded virtual state mechanism	20050505	718/1
US 20050086565 A1	System and method for generating a test case	20050421	714/741
US 20050081113 A1	Method and apparatus for analyzing digital circuits	20050414	714/39
US 20050071145 A1	Simulation apparatus, simulation program, and recording medium	20050331	703/19
US 20050034088 A1	Method and apparatus for mapping platform-based design to multiple foundry processes	20050210	716/4
US 20050034087 A1	Method and apparatus for mapping platform-based design to multiple foundry processes	20050210	716/3
US 20050034086 A1	Method and apparatus for mapping platform-based design to multiple foundry processes	20050210	716/3
US 20050027891 A1	Integrated circuit with a scalable high-bandwidth architecture	20050203	709/253
US 20050023656 A1	Vertical system integration	20050203	257/678
US 20050021986 A1	Apparatus and method for memory encryption with reduced decryption latency	20050127	713/193
US 20040268050 A1	Apparatus and method for an adaptive multiple line prefetcher	20041230	711/137
US 20040267996 A1	Queued locks using monitor-memory wait	20041230	710/200
US 20040260993 A1	Method, system, and program for simulating Input/Output (I/O) requests to test a system	20041223	714/743
US 20040259564 A1	Optimal load-based wireless session context transfer	20041223	455/453
US 20040252701 A1	Systems, processes and integrated circuits for rate and/or diversity adaptation for packet comi	20041216	370/395.21
US 20040250150 A1	Devices, systems and methods for mode driven stops notice	20041209	713/330
US 20040236876 A1	Apparatus and method of memory access control for bus masters	20041125	710/22
US 20040236564 A1	Simulation of a PCI device's memory-mapped I/O registers	20041125	703/25
US 20040216076 A1	METHOD, SYSTEM AND PROGRAM PRODUCT FOR UTILIZING A CONFIGURATION DAT/	20041028	716/18
US 20040215441 A1	Applying constraints to block diagram models	20041028	703/22
US 20040215434 A1	Method, system and program product for configuring a simulation model of a digital design	20041028	703/15
US 20040199878 A1	Method and apparatus for automated synthesis of multi-channel circuits	20041007	716/1
US 20040193957 A1	Emulation devices, systems and methods utilizing state machines	20040930	714/30
US 20040193394 A1	Method for CPU simulation using virtual machine extensions	20040930	703/22
US 20040168137 A1	Use of time step information in a design verification system	20040826	716/5
US 20040158788 A1	Method for functional verification of an integrated circuit model in order to create a verification p	20040812	714/741
US 20040128563 A1	Mechanism for processor power state aware distribution of lowest priority interrupt	20040701	713/300
US 20040128416 A1	Apparatus and method for address bus power control	20040701	710/107
US 20040124874 A1	Apparatus and method for bus signal termination compensation during detected quiet cycle	20040701	326/30
US 20040117756 A1	Methods and apparatuses for designing integrated circuits	20040617	716/18
US 20040117671 A1	Apparatus and method for address bus power control	20040617	713/300
US 20040117670 A1	Apparatus and method for data bus power control	20040617	713/300
US 20040103330 A1	Adjusting voltage supplied to a processor in response to clock frequency	20040527	713/322
US 20040083475 A1	Distribution of operations to remote computers	20040429	718/102
US 20040064814 A1	System and method for task arbitration in multi-threaded simulations	20040401	718/100
US 20040044510 A1	Fast simulaton of circuitry having soi transistors	20040304	703/14
US 20040024578 A1	Discrete event simulation system and method	20040205	703/17
US 20040015808 A1	System and method for providing defect printability analysis of photolithographic masks with jol	20040122	716/19
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US 20030229483 A1	Causality based event driven timing analysis engine	20031211	703/19

US 20030225556 A1	Apparatus and method for connecting hardware to a circuit simulation	20031204	703/14
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US 20030208488 A1	System and method for organizing, compressing and structuring data for data mining readines:	20031106	707/6
US 20030204389 A1	Method for numerically simulating an electrical circuit	20031030	703/19
US 20030200425 A1	Devices, systems and methods for mode driven stops	20031023	712/229
US 20030196144 A1	Processor condition sensing circuits, systems and methods	20031016	714/34
US 20030188302 A1	Method and apparatus for detecting and decomposing component loops in a logic design	20031002	717/160
US 20030188299 A1	Method and apparatus for simulation system compiler	20031002	717/141
US 20030187853 A1	Distributed data storage system and method	20031002	707/10
US 20030149954 A1	Methods and apparatuses for designing integrated circuits	20030807	716/18
US 20030144828 A1	Hub array system and method	20030731	703/21
US 20030130833 A1	Reconfigurable, virtual processing system, cluster, network and method	20030710	703/23
US 20030130832 A1	Virtual networking system and method in a processing system	20030710	703/23
US 20030126454 A1	Authenticated code method and apparatus	20030703	713/193
US 20030126453 A1	Processor supporting execution of an authenticated code instruction	20030703	713/193
US 20030126442 A1	Authenticated code module	20030703	713/170
US 20030126416 A1	Suspending execution of a thread in a multi-threaded processor	20030703	712/235
US 20030126379 A1	Instruction sequences for suspending execution of a thread until a specified memory access oc	20030703	711/150
US 20030126375 A1	Coherency techniques for suspending execution of a thread until a specified memory access o	20030703	711/145
US 20030126186 A1	Method and apparatus for suspending execution of a thread until a specified memory access o	20030703	718/107
US 20030126059 A1	Intelectual property (IP) brokering system and method	20030703	705/36
US 20030125913 A1	Linear time invariant system simulation with iterative model	20030703	703/2
US 20030125907 A1	Monitor, system and method for monitoring performance of a scheduler	20030703	702/186
US 20030115569 A1	Method and system for optical proximity correction	20030619	716/19
US 20030101040 A1	Hardware simulation using a test scenario manager	20030529	703/17
US 20030093569 A1	Synchronization of distributed simulation nodes by keeping timestep schedulers in lockstep	20030515	709/248
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US 20030093253 A1	Grammar for message passing in a distributed simulation environment	20030515	703/13
US 20030079195 A1	Methods and apparatuses for designing integrated circuits	20030424	716/8
US 20030079093 A1	Server system operation control method	20030424	711/147
US 20030061580 A1	Simulation method and compiler for hardware/software programming	20030327	716/4
US 20030037305 A1	Method and apparatus for evaluating logic states of design nodes for cycle-based simulation	20030220	716/4
US 20030036894 A1	Method and apparatus for amortizing critical path computations	20030220	703/19
US 20030009467 A1	System and method for organizing, compressing and structuring data for data mining readines:	20030109	707/100
US 20020194572 A1	Methods and apparatuses for designing integrated circuits	20021219	716/1
US 20020183054 A1	Mobile system testing architecture	20021205	455/423
US 20020156613 A1	Service clusters and method in a processing system with failover capability	20021024	703/23
US 20020156612 A1	Address resolution protocol system and method in a virtual network	20021024	703/23
US 20020152060 A1	Inter-chip communication system	20021017	703/17
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US 20020144214 A1	Apparatus for optimized constraint characterization with degradation options and associated m	20021003	716/2
US 20020144183 A1	Microprocessor design support for computer system and platform validation	20021003	714/37
US 20020143516 A1	Apparatus and methods for constraint characterization with degradation options	20021003	703/19
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US 20020124217 A1	Testing apparatus and testing method for an integrated circuit, and integrated circuit	20020905	714/726
US 20020124085 A1	Method of simulating operation of logical unit, and computer-readable recording medium retain	20020905	709/226
US 20020101824 A1	System and method for connecting a logic circuit simulation to a network	20020801	370/241
US 20020099455 A1	Programmable controller	20020725	700/83
US 20020087913 A1	System and method for performing automatic rejuvenation at the optimal time based on work l	20020704	714/15
US 20020073375 A1	Method and apparatus for test generation during circuit design	20020613	714/739
US 20020052725 A1	Distributed simulation	20020502	703/22
US 20020049576 A1	Digital and analog mixed signal simulation using PLI API	20020425	703/14
US 20020042704 A1	Apparatus and methods for characterizing electronic circuits having multiple power supplies	20020411	703/14
US 20020022971 A1	Software rental system, software rental method, and computer program for being executed on	20020221	705/1
US 20020013918 A1	Devices, systems and methods for mode driven stops	20020131	714/30
US 20010056341 A1	Method and apparatus for debugging programs in a distributed environment	20011227	703/22
US 20010037424 A1	Snoop phase in a highly pipelined bus architecture	20011101	710/220
US 20010037421 A1	Enhanced highly pipelined bus architecture	20011101	710/305
US 20010027386 A1	TIME-DOMAIN CIRCUIT MODELLER	20011004	703/14
US 6922740 B2	Apparatus and method of memory access control for bus masters	20050726	710/22
US 6920418 B2	Detecting events within simulation models	20050719	703/17
US 6918103 B2	Integrated circuit configuration	20050712	716/18
US 6917909 B1	Facilitating guidance provision for an architectural exploration based design creation process	20050712	703/14
US 6909330 B2	Automatic phase lock loop design using geometric programming	20050621	331/8
US 6907487 B2	Enhanced highly pipelined bus architecture	20050614	710/305
US 6880069 B1	Replay instruction morphing	20050412	712/227
US 6880031 B2	Snoop phase in a highly pipelined bus architecture	20050412	710/305
US 6879948 B1	Synchronization of hardware simulation processes	20050412	703/14
US 6842035 B2	Apparatus and method for bus signal termination compensation during detected quiet cycle	20050111	326/30
US 6832298 B2	Server system operation control method	20041214	711/147
US 6826732 B2	Method, system and program product for utilizing a configuration database to configure a hard\	20041130	716/1
US 6820215 B2	System and method for performing automatic rejuvenation at the optimal time based on work l	20041116	714/15
US 6816732 B1	Optimal load-based wireless session context transfer	20041109	455/453
US 6810442 B1	Memory mapping system and method	20041026	710/22
US 6807520 B1	System and method for simulation of an integrated circuit design using a hierarchical input netli	20041019	703/14
US 6804735 B2	Response and data phases in a highly pipelined bus architecture	20041012	710/112
US 6785873 B1	Emulation system with multiple asynchronous clocks	20040831	716/4
US 6772370 B1	Method and apparatus for generation of pipeline hazard test sequences	20040803	714/33
US 6769122 B1	Multithreaded layered-code processor	20040727	718/102
US 6760866 B2	Process of operating a processor with domains and clocks	20040706	714/34
US 6754763 B2	Multi-board connection system for use in electronic design automation	20040622	710/317
US 6751759 B1	Method and apparatus for pipeline hazard detection	20040615	714/55
US 6704895 B1	Integrated circuit with emulation register in JTAG JAP	20040309	714/726

US 6668364 B2	Methods and apparatuses for designing integrated circuits	20031223	716/7
US 6651225 B1	Dynamic evaluation logic system and method	20031118	716/4
US 6651038 B1	Architecture for simulation testbench control	20031118	703/27
US 6606734 B2	Simulation method and compiler for hardware/software programming	20030812	716/4
US 6584598 B2	Apparatus for optimized constraint characterization with degradation options and associated m	20030624	716/2
US 6581019 B1	Computer-system-on-a-chip with test-mode addressing of normally off-bus input/output ports	20030617	702/120
US 6549881 B1	Interface for interfacing simulation tests written in a high-level programming language to a simu	20030415	703/21
US 6546505 B1	Processor condition sensing circuits, systems and methods	20030408	714/30
US 6542483 B1	Method and an apparatus for Eb/Nt estimation for forward power control in spread spectrum c	20030401	370/332
US 6539497 B2	IC with selectively applied functional and test clocks	20030325	714/30
US 6530065 B1	Client-server simulator, such as an electrical circuit simulator provided by a web server over th	20030304	716/4
US 6530054 B2	Method and apparatus for test generation during circuit design	20030304	714/739
US 6522985 B1	Emulation devices, systems and methods utilizing state machines	20030218	702/117
US 6519754 B1	Methods and apparatuses for designing integrated circuits	20030211	716/18
US 6498999 B1	Method and apparatus for design verification of an integrated circuit using a simulation test ben	20021224	702/120
US 6490642 B1	Locked read/write on separate address/data bus using write barrier	20021203	710/110
US 6470482 B1	METHOD AND SYSTEM FOR CREATING, DERIVING AND VALIDATING STRUCTURAL DE	20021022	716/6
US 6466898 B1	Multithreaded, mixed hardware description languages logic simulation on engineering workstati	20021015	703/17
US 6460167 B1	Efficient system for multi-level shape interactions	20021001	716/4
US 6449578 B1	Method and apparatus for determining the RC delays of a network of an integrated circuit	20020910	702/119
US 6438735 B1	Methods and apparatuses for designing integrated circuits	20020820	716/7
US 6421251 B1	Array board interconnect system and method	20020716	361/788
US 6389498 B1	Microprocessor having addressable communication port	20020514	710/268
US 6389379 B1	Converification system and method	20020514	703/14
US 6370679 B1	Data hierarchy layout correction and verification method and apparatus	20020409	716/19
US 6349392 B1	Devices, systems and methods for mode driven stops	20020219	714/30
US 6347388 B1	Method and apparatus for test generation during circuit design	20020212	714/739
US 6345242 B1	Synchronization mechanism for distributed hardware simulation	20020205	703/22
US 6321366 B1	Timing-insensitive glitch-free logic system and method	20011120	716/6
US 6314552 B1	Electronic design creation through architectural exploration	20011106	716/18
US 6314389 B1	Time-domain circuit modeller	20011106	703/14
US 6305006 B1	Generating candidate architectures for an architectural exploration based electronic design cre	20011016	716/18
US 6292764 B1	Tunable architecture for device adapter	20010918	703/14
US 6263484 B1	Prototyping system and a method of operating the same	20010717	716/18
US 6263303 B1	Simulator architecture	20010717	703/19
US 6216252 B1	Method and system for creating, validating, and scaling structural description of electronic devi	20010410	716/1
US 6212667 B1	Integrated circuit test coverage evaluation and adjustment mechanism and method	20010403	716/6
US 6212493 B1	Profile directed simulation used to target time-critical crossproducts during random vector testi	20010403	703/22
US 6182258 B1	Method and apparatus for test generation during circuit design	20010130	714/739
US 6169992 B1	Search engine for remote access to database management systems	20010102	707/103R
US 6154719 A	Logic simulation system and method	20001128	703/13
US 6134516 A	Simulation server system and method	20001017	703/27
US 6117182 A	Optimum buffer placement for noise avoidance	20000912	716/8

US 6117181 A	Synchronization mechanism for distributed hardware simulation	20000912	703/22
US 6085336 A	Data processing devices, systems and methods with mode driven stops	20000704	714/30
US 6077304 A	Verification system for simulator	20000620	703/14
US 6047387 A	Simulation system for testing and displaying integrated circuit's data transmission function of pe	20000404	714/33
US 6032268 A	Processor condition sensing circuits, systems and methods	20000229	714/30
US 6026230 A	Memory simulation system and method	20000215	703/13
US 6014512 A	Method and apparatus for simulation of a multi-processor circuit	20000111	703/27
US 6009256 A	Simulation/emulation system and method	19991228	703/13
US 5966537 A	Method and apparatus for dynamically optimizing an executable computer program using input	19991012	717/158
US 5960186 A	Digital circuit simulation with data interface scheduling	19990928	703/4
US 5911059 A	Method and apparatus for testing software	19990608	703/23
US 5907698 A	Method and apparatus for characterizing static and dynamic operation of an architectural syste	19990525	716/6
US 5905883 A	Verification system for circuit simulator	19990518	703/17
US 5878246 A	System for linking an interposition module between two modules to provide compatibility as mc	19990302	703/27
US 5867689 A	Method and apparatus for emulating a digital cross-connect switch network using a flexible topo	19990202	703/23
US 5867399 A	System and method for creating and validating structural description of electronic system from	19990202	716/18
US 5850536 A	Method and system for simulated multi-tasking	19981215	703/21
US 5848236 A	Object-oriented development framework for distributed hardware simulation	19981208	714/33
US 5841670 A	Emulation devices, systems and methods with distributed control of clock domains	19981124	703/23
US 5812826 A	Method and apparatus for emulating a network of state monitoring devices	19980922	703/27
US 5812824 A	Method and system for preventing device access collision in a distributed simulation executing i	19980922	703/14
US 5809286 A	Method and apparatus for emulating a dynamically configured digital cross-connect switch netv	19980915	703/23
US 5805792 A	Emulation devices, systems, and methods	19980908	714/28
US 5801958 A	Method and system for creating and validating low level description of electronic design from hi	19980901	716/18
US 5764948 A	Method and apparatus for determining a composition of an integrated circuit	19980609	716/17
US 5748617 A	Method and apparatus for emulating a digital cross-connect switch network	19980505	370/244
US 5737583 A	Digital circuit simulation	19980407	703/14
US 5732247 A	Interface for interfacing simulation tests written in a high-level programming language to a simu	19980324	703/13
US 5701439 A	Combined discrete-event and continuous model simulation and analysis tool	19971223	703/17
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US 5623418 A	System and method for creating and validating structural description of electronic system	19970422	716/1
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US 5594741 A	Method for control of random test vector generation	19970114	714/741
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US 5553276 A	Self-time processor with dynamic clock generator having plurality of tracking elements for outpu	19960903	713/500
US 5546562 A	Method and apparatus to emulate VLSI circuits within a logic simulator	19960813	703/14
US 5544342 A	System and method for prefetching information in a processing system	19960806	711/119
US 5544067 A	Method and system for creating, deriving and validating structural description of electronic syst	19960806	703/14
US 5535331 A	Processor condition sensing circuits, systems and methods	19960709	714/45
US 5493672 A	Concurrent simulation of host system at instruction level and input/output system at logic level v	19960220	703/21
US 5490096 A	Visual simulation apparatus	19960206	703/13
US 5437037 A	Simulation using compiled function description language	19950725	717/146

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US 5371851 A	Graphical data base editor	19941206	345/501	
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US 5072378 A	Direct access storage device with independently stored parity	19911210	714/6	
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US 4878179 A	Interactive diagnostic methodology and apparatus for microelectronic devices	19891031	716/4	
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